Paul George

Email : command.paul@gmail.com
Mobile : +91-99-104-74414

Education

- **Shiv Nadar University** — Dadri, UP, India
  Bachelor of Technology in Electronics and Communication Engineering ; GPA: 7.69/10 — *Aug. 2014 – May. 2018*
  - **Relevant Coursework**: Digital System Design With FPGAs, Embedded Systems Hardware, Operating Systems, Data Structures & Algorithms, Digital Signal Processing, Applied Machine Learning, Brain Sciences and Cognition, Communication Engineering, Computer Networks, Mathematical Methods, Control Systems, Electromagnetic Engineering, VLSI Technology and Design, Design of Analog CMOS Circuits, Information Theory& Coding, Network Analysis.

- **IIT Madras - Pennsylvania State University - MHRD-GIAN Course** — Chennai, TN, India
  Short Term Course :: Emerging Computational Devices, Architectures and Computational Models — *December 2017*

Experience

- **RISE-Group IIT MADRAS** — Chennai, TN, India
  Project Associate - Ministry of E&IT - India Microprocessor Development Program,Intern(2017) — *May 2017 - Present*
  - **Shakti-Thales Group: Safe RV**: Octa-Core Criticality Aware Network On-Chip Enabled SoC Implementing a Directory-Based MSI Coherence Protocol for an Integrated Avionics Multiprocessing System. Developed components: TileLink-C Fabric & Transactors , Criticality enabled OpenSmart Network on-chip Interface Controller, performance monitoring virtual network and Many-Core Debug - Presented at the RISC-V Summit - San Jose 2019 & Shakti Week 2019.
  - **Shakti TLS - Fault-Tolerant Core Complex**: Design and Development of a Re-configurable Fault-Tolerant Core Complex, Implementing degradable Triple Modular Redundancy(Triple Lock Step), ECC protected storage elements, and Watchdog Timer guarded FSMs.
  - **Debug Subsystem**: Designed in Bluespec SV a RISC-V Debug spec 0.14 Draft compliant Debugger and JTAG TAPC used in The Shakti RISE-CREEK(Intel 22nm) & Shakti Rimo (ISRO-SCL 180nm) Test Chips, Compatible with Shakti C/E/I Class Pipelines.
  - **Formal Specification**: Formal Specification and Synthesis of an ECC Encoder-Decoder pair using the Kami(MIT-PLV) Framework in COQ(INRIA), Evaluation of Other RISC-V Formal Model Candidates.
  - **Shakti Lock Step Verification Framework**: Bachelors Thesis Project. Advisors: Prof. R.N.Biswas, Dr Neel Gala. Extensible Functional Verification Framework for RISC-V compliant cores - Presented At the 2018 - RISC-Workshop - IIT Madras.
  - **Misc.**: Post Silicon Validation and Bring up for Shakti-RISE-CREEK Shakti-RIMO Test Chips. Clock Recovery IP for Custom Off Chip Memory Interface. Custom TAP Controller for ShaktiSoc Arty FPGA Evaluation Package.
  - **RISCV- Foundation**: Member Technical committee (sponsored by IIT Madras)- Formal Specification, Memory Model & Trace subgroups.

- **Shiv Nadar University** — Dadri, UP, India
  Undergraduate Research and Teaching Assistant — *May 2016 - Dec 2017*
  - **RNBIP**: Developed an 8 Bit Pipelined Processor-FPGA Proven, Developed an Emulator for verification and use as a teaching aid. Has been used in 3 iterations of Prof. R.N.Biswas's Digital Design and Embedded systems courses since 2016.
  - **SNU - Center for Urban Studies and Disaster Management**: Explored the Feasibility of a crowd-sourced Earthquake Early Warning System with Smartphones, low-cost edge sensors & a Cloud Monitor context specific to the Indian Sub-Continent. Designed and Fabricated Prototype Sensor Modules, Trained a Decision Tree Classifier for P-Wave Identification with Hand Crafted Feature Set. Interacted with the Ministry of Earth Sciences (GOI). Presented a Poster at the ASCE - International Sustainability Conference 2017.

- **HCL Infosystems LTD.** — Sedarapet, Puducherry , India
  Summer Intern — *May 2015 - July 2015*
  - **Multiple Products**: IoT Enabled embedded solutions for customers in the automotive and healthcare sector using TI/STM ARM Micro-Controllers and Misc Radios/Sensors.

Projects

- **A Feasibility Study of Flapping Wing Actuation using Dielectric Elastomers**: I developed a Low-Cost apparatus for High Voltage (20kv) Function Generation and Measurement for use in evaluating Dielectric Elastomers. Derived an electrical model from experimental Data and Validated the same in SPICE — presented Work at ESMT-2018 - Osaka, Japan.
- **BLIP - Bluetooth Based Indoor Positioning - India Hacks 2016**: Open Source Project Developed enabling context-based services and asset tracking in indoor spaces(1M Accuracy). Placed 7th/27000 Teams at a Hackathon.
- **Electro-Myography and Activity Tracking**: Course Project: Developed a Multi-Channel Wireless Electro-Myograph. Activity Classifier implemented in Matlab for use with motion capture / VR systems.

Technical Skills

- **Technologies**: Bluespec SV, Verilog, Synthesis Asic-(DC/Genus), FPGA - Xilinx, MIT-Kami, Z3, Racket, ASM(RISCV) C, C++, Python, Linux, GDB, Valgrind, OpenOCD, Matlab, TensorFlow, KICAD , CST EMS, Virtuoso , SPICE , CUDA, OPEN MPI, OPEN MP, LaTeX